A Ka-Band Quasi-F^{-1} Power Amplifier in a 130 nm SiGe BiCMOS Technology

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***Abstract*—In this paper the design, analysis and implementation of a single-stage, 2nd-harmonically tuned, quasi-inverse class F power amplifier, suitable for mm-wave 5G applications is presented. A detailed methodology for the discovery of the active device's output capacitance is analyzed leading to optimized performance. The PA is integrated in a $0.13\,\mu m$ SiGe BiCMOS technology with $f_T/f_{max} = 250/370\,GHz$, achieving a power-added efficiency $PAE > 30$ %, a saturation output power $P_{sat} > 18\,dBm$ and a maximum large-signal power gain $G_p > 14\,dB$, in the frequency band $37 - 40\,GHz$. The chip size is $0.605 \times 0.712\,mm^2$ including all pads.**

***Index Terms*—Cascode amplifier, inverse class F, quasi-F^{-1}, harmonic tuned PA, mm-wave amplifier, power amplifier, 38 GHz.**

I. Introduction

The ever increasing demand for high data rates and lower latency driven by consumer demand for mobile data, improved performance, quality and reliability as well as the emerge of 5G enhanced mobile broadband applications (eMBB) boost Federal Communication Committee (FCC) to announce procedures for mm-wave auctions [1]. One of the mm-wave frequency bands of interest is the 37-40 GHz range, where the proposed power amplifier is operating [2].

Critical part of the mm-wave transmitter chain, in terms of power consumption and linearity, is the Power Amplifier (PA) [3]. Highly efficient silicon mm-wave PAs, able to provide reasonable PAE at power back-off (PBO), is challenging not only due to inherent trade-off between break-down voltages and maximum speed in silicon-based transistors, but also because of a limited Q from the integrated passive components [4]. In this sense, further investigation of PA modeling could enforce the accurate designing of digital or analog pre-distorters, envelope tracking and linear Doherty PAs [5].

In this brief, a new technique for the designing of a harmonically tuned PA is proposed. Assuming that the model of our PA's active device (AD) comprises an input and output impedance as well as a current generator, necessary part of this technique is the discovery of the output capacitance of the active device, described in Section II. A brief design analysis for the fabricated PA is summarized in Section III, while a simple model for the voltage and current waveform plotting after the extraction of the parasitic output capacitance is shown in Section IV. Simulation and experimental validation of the proposed PA is denoted in Section V.

II. Evaluation Of The Output Capacitance C_{out}

A precise modeling of a mm-wave PA is incident to the accurate modeling of its main amplifying core or active module of each stage and the EM characterization of its passive structures. Considering the active module as a voltage depended current source with an input and output admittance $Y_{in} = G_{in} + jB_{in}$ and $Y_{out} = G_{out} + jB_{out}$ respectively (Figure 1a), a "loop gain" analysis can be performed at node X, not only for stability inspection but also for the Y_{out} estimation. In this sense, by "breaking" the circuit at the desired node, without affecting the overall performance, the imitation of the "loop gain" process could lead in finding the output admittance Y_{out}. Such an analysis would be beneficial to the circuit design flow, especially for multiple-stage PAs with or without feedback loops (Figure 1b), in contrast to the conventional Large-signal S-parameter analysis (LSSP) which fails to provide information about the input and output impedances of the intermediate stages.

Figure 1c shows the amplifying core model of the proposed single-stage PA which approaches the cascode topology as a unique active device. Isolating the AD from the output matching network (OMN), the output capacitance C_{out} can be extracted as:

$$C_{out} = B_{out}/\omega \qquad (1)$$

where ω is the angular frequency. The ideal rf choke provides a transparent dc current path.

As follows, we are able to extract the input and output impedances of the device under test while the driving power at the input of the device is being swept. Thus, the variations of the device's output capacitance with reference to its driving power can be easily captured, enforcing the accuracy of the designing process.

The simulation results of the harmonic balance "loop gain" analyses at the operating frequency range of $37 - 40\,GHz$, are denoted in Fig. 2, where the output capacitance C_{out} of our active device over the input power P_{in} sweep is shown. Ideal conjugate matching is used at the input of our active device while a 15Ω resistor is inserted in the base of the common-emitter (CE) HBT Q_1, in order for our active device to become stable at the frequency band of interest. Our results denote that C_{out} is approximately $115\,fF$ when our active device is driven by low input power, while at the operating point where the power gain is 1-dB compressed ($\sim 4 - 5\,dBm$), C_{out} equals $120 - 125\,fF$.

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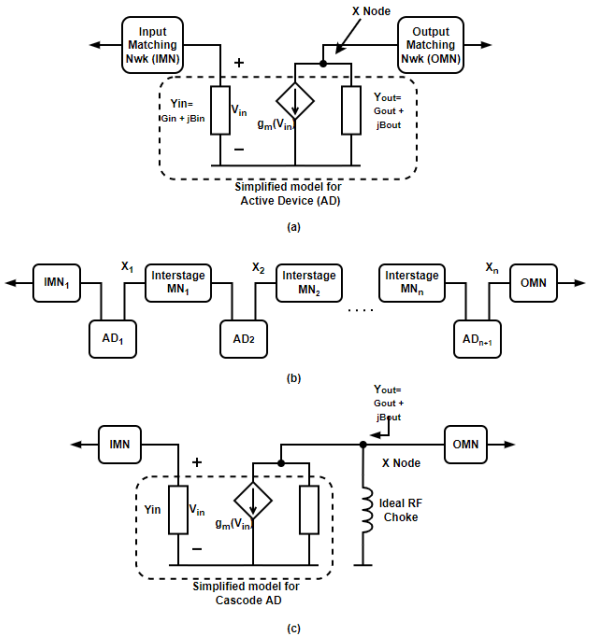

Fig. 1. (a) Simplified model for a PA's active device and X node notation. (b) X nodes of a multiple-stage PA. (c) Simplified model for the cascode AD of the proposed PA.

Fig. 2. Output capacitance C_{out} vs the available input power P_{in}.

These results can be easily verified if the extracted output capacitance is cancelled by the required inductance:

$$L_{req} = \frac{1}{\omega^2 C_{out}} \tag{2}$$

Performing a swept power Load Pull analysis at $38GHz$, the power contours at the $IP_{1dB} = 5\ dBm$ compression point are centered around the impedance $Z_{Load} = 13.9 + j22.4\ \Omega$. Replacing the rf choke component with an ideal inductance of $\sim 146\ pH$, the load pull contours are centered at the real axis, around the optimum load $Z_{Load}{}' = 50 + j0\ \Omega$, exactly as it is shown in Fig.3 and mentioned in [4]. Mathematically, the load impedance transition can be proven via the well-known equations for the series to parallel impedance conversion:

$$\begin{cases} Z_{Load} = R_S + jX_S & (3) \\ Y_{Load} = \dfrac{1}{R_P} - j\dfrac{1}{X_P} \xrightarrow{with\ Cout\ canc.} Y_{Load}{}' = \dfrac{1}{R_P} & (4) \\ Q = \dfrac{X_S}{R_S} = \dfrac{R_P}{X_P} & (5) \end{cases}$$

$$\Leftrightarrow Z_{Load}{}' = \frac{1}{Y_{Load}{}'} + j0 = R_P = (Q^2+1)\cdot R_S \tag{6}$$

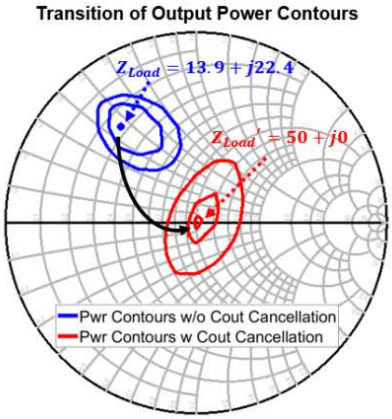

Fig. 3. Power contours w & w/o C_{out} cancellation. The power stepis 0.5 dBm.

Keeping as reference the Load Pull analysis for the validation of the discovery process of C_{out}, it is worth mentioning that the aforementioned method based on the loop gain analysis of a single Harmonic Balance (HB) simulation gave us more accurate results in contrast with the traditional large-signal s-parameter (LSSP) simulation. The proposed novel method for C_{out} investigation gives the opportunity for precise modeling of harmonically tuned and highly efficient PA classes, such as Class-F, F-1, E [6].

III. Quasi-Inverse Class F Power Amplifier

Figure 4 shows the proposed single-stage, second-harmonically tuned, $37-40\ GHz$, quasi-F^{-1} Power Amplifier. The designed quasi-F^{-1} PA imitates the behavior of a conventional inverse class F PA concerning the harmonically tuned output termination. The difference of the proposed PA class is that it controls only the 2nd harmonic of the output voltage across the active device simplifying the design of the output matching network. In conventional inverse class F PAs the additional 3rd harmonic resonator of the output current inserts extra losses in such a high frequency operation, often cancelling the desired efficiency enhancement, due to limited Q of the passive components [4].

The suggested design consists of a cascode topology as the selected active device, a simple but effective cascode current mirror as a bias network and a T-type input matching network. Moreover, the proposed PA schematic adopts an output harmonically tuned load in order to provide an optimum 50-Ω fundamental impedance and an open circuit second harmonic load. The terminated impedance at both the input and output port is $50\ \Omega$.

The presented quasi-F^{-1} PA is designed and fabricated in Infineon's 130 nm SiGe BiCMOS process. The process features high-speed NPN HBTs with $f_T/f_{max} = 250/370\ GHz$. The layer stackup profile includes 6 copper metal layers (one thick) and $1.0\ \mu m$ aluminum layer as top metal.

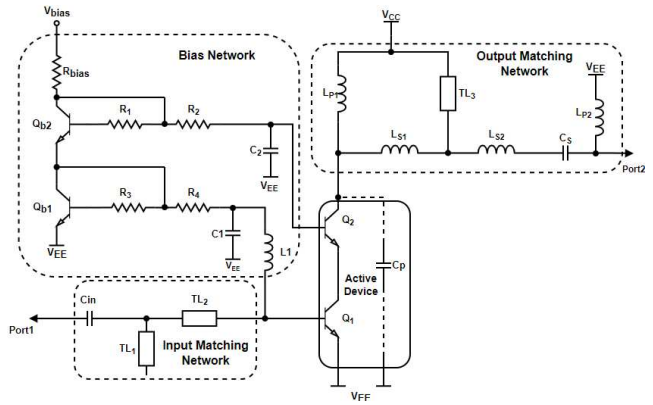

Fig. 4. Schematic of the proposed single-stage quasi-F^{-1} PA.

A. Cascode Topology

Cascode topology is selected as our main amplifying core. The main advantages of the cascode topology, impelled us for selection, are the higher gain and the reduction of the Miller's effect enforcing the active device's stability [7], [8].

The size of $Q_{1,2}$ is selected in such a way, so as to achieve an output saturated power delivered to the load more than 18 dBm, when it is biased in a deep class AB point. Such a bias point, referred as sweet spot [9], makes the biased HBT produce a maximum current at the first harmonic, similar to that when it is biased into a class A point. Moreover, biasing an HBT in a deep class AB point reduces the maximum collector current of the third harmonic substantially, as it is mentioned in [7]. The bases of $Q_{1,2}$ is biased at $\sim 0.81\,V$ and $\sim 1.65\,V$ respectively, leading the cascode branch to conduct$\sim 12\,mA$ of quiescent collector current. The overall emitter length of the selected double emitter HBTs (CBEBEBC) is $l_e = 6\,bl \times 2 \times 2.8\mu m$ and it is optimized to have a current density of $J_C \approx 11.5\ mA/\mu m^2$ achieving a peak $250\,GHz$ f_T at $18.6\,dBm$ OP_{-1dB} ($I_{DC} = 51\,mA$). This maintains $\sim 16\,dB$ power gain at 38 GHz until the output reaches 1-dB gain compression point.

B. Output Matching Network

The implementation of the proposed OMN is based on [10] and adopts a harmonically tuned circuitry offering a transparent current path for the first harmonic as well as an effective short circuit of the second harmonic.

In order to calculate the ideal values of the components that constitute the output network, it is necessary to determine the parasitic capacitance C_p of the active device. C_p can be easily extracted and verified from the methodology described in Section II. Inductor L_{P1} resonates the parasitic capacitance $C_p$transferring the optimum load impedance, close to the real axis of the Smith Chart.

After the extraction of C_p, the process for the calculation of the ideal inductances and capacitances of the output matching network are straightforward. At the fundamental operating frequency f_0, the short-circuit termination at the one end of the quarter wavelength line $(\lambda/4)\,TL_3$ becomes transformed into an open circuit at the other end. Thus, the OMN becomes a shunt L_{P1}-C_p tank in series with $L_S = L_{S1} + L_{S2}$, and C_S, realizing a dual f_0 resonator (Fig. 5a). It should be mentioned that the inductor L_{P2} cancels out the parasitic capacitance $C_{PAD} \approx 20\,fF$, that the output rf pad exhibits. The inductor L_{P1} resonates out the parasitic capacitance C_p, while the series resonator L_s, C_s provides a transparent fundamental current path from the generator device (Q_1, Q_2) to our 50 Ω load.

TABLE I
PASSIVE COMPONENTS OF THE OMN

C_p, C_S	L_{P1}	L_{S1}	L_{S2}	C_{PAD}	L_{P2}
$120\,fF$	$146\,pH$	$49\,pH$	$97\,pH$	$20\,fF$	$877\,pH$

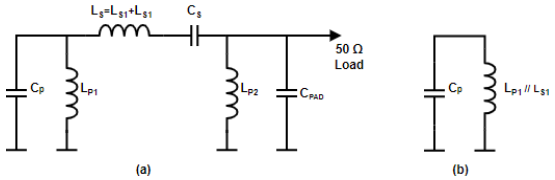

Fig. 5. Schematic of the output-circuit at (a) the fundamental, (b) second harmonic.

At the second harmonic, the quarter wavelength line becomes short, isolating the PA from the output load. As shown in Figure 5b, this effectively transforms the load network to a parallel second harmonic resonator, composed of L_{P1} in parallel with L_{S1} and C_p, providing the transistors of the active device with a high impedance at the second harmonic ($Z_2 = \infty$). Table I summarizes the values of the passive components of the OMN, used in the present work.

IV. INTRINSIC VOLTAGE & CURRENT WAVEFORMS

Time domain intrinsic collector current and voltage waveforms, after the cancellation of the parasitic capacitance C_{out} can give us an overview concerning the active device's performance that it is connected to a harmonically tuned load. Figure 6 shows the schematic model we used in order to extract the voltage and current waveforms at the output of the cascode topology, as we not have access to the intrinsic current source node of the provided HBT model. The key parts of our model are a multitone voltage source that represents the magnitude and phase components of the voltage (extracted from a HB analysis) at the collector node of the common base HBT Q_2 and an ideal capacitor C_{out} that imitates the behavior of the active device's output parasitic capacitance over frequency. In our design, C_{out} changes $< 4\,\%$ at higher harmonics, so we selected a constant capacitance $C_{out} = 120\,fF$ to simplify our model.

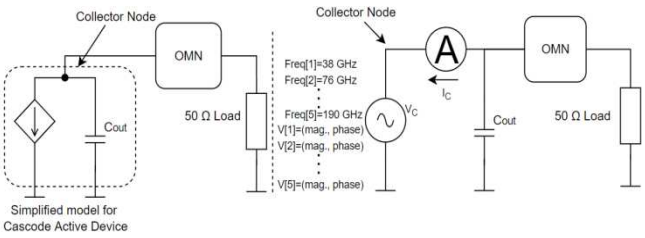

Fig. 6. Simplified model for the extraction of the time-domain collector voltage and current waveforms.

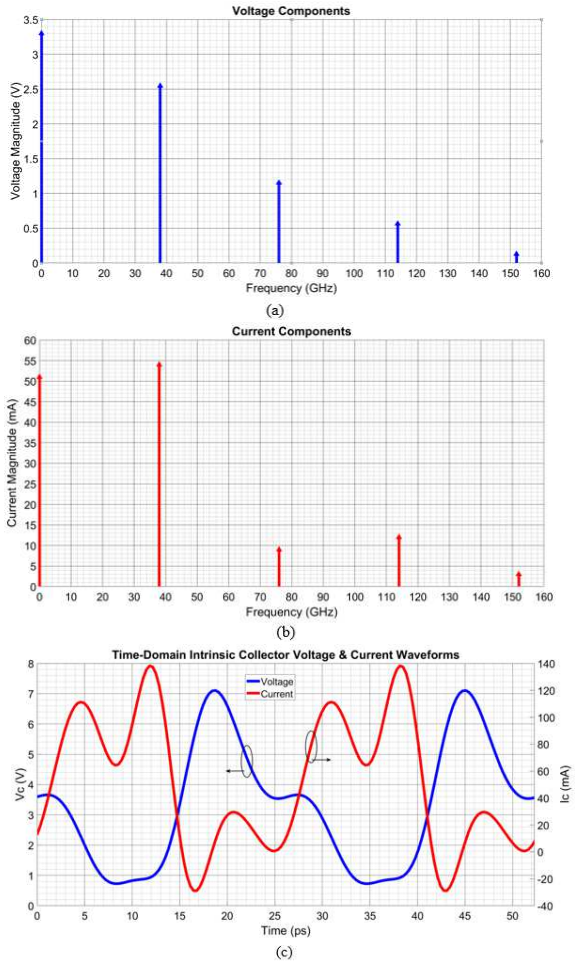

Fig. 7. Simulated collector voltage (a) and current (b) in frequency domain and in time domain (c).

The interposed amperemeter between the voltage source and the parallel combination $C_{out}//OMN$ measures the intrinsic current of our active topology. For an accurate plotting of the two waveforms, an addition of the V-I dc components is required. The time domain collector current and voltage waveforms at the operating point of 1-dB gain compression point at 38 GHz is shown in Figure 7c and corresponds to a PAE performance of ~40%. The strong 2nd harmonic of the intrinsic collector voltage (Fig. 7a) leads to a half-sinusoidal waveform approximation, while the weak and moderate 2nd and 3rd components of the current, form an approximately square waveform (Fig. 7b). These two waveforms imply reduced V-I overlapping and thus enhanced efficiency.

V. Simulation & Measurement Results

Figure 8 shows the photograph of the fabricated chip. The chip area is $0.605 \times 0.712\ mm^2$ including all pads. Our class quasi-F^{-1} power amplifier was measured on a probe station. Small and large signal measurements were performed via a VNA and a microwave analog signal generator in combination with a power sensor, respectively. RF cable loss was characterized and de-embedded, over the desired frequency range.

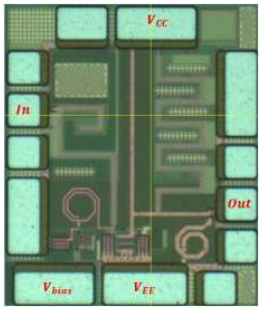

Fig. 8. Chip photograph.

Figure 9 shows the small-signal S-parameter measurement and simulation results of our PA ($V_{CC}/V_{bias} = 3.3/2.1\ V, I_{DC} = 12\ mA$). The measured $S21$ is higher than 13 dB for the frequency range $37 - 40\ GHz$ with the peak of 15.6 dB at 37 GHz, while the $S11 < -15\ dB$ over $38 - 40\ GHz$. The PA is stable over the entire frequency range.

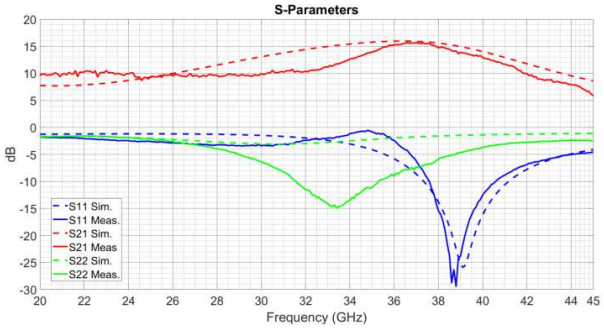

Fig. 9. Small-Signal S-Parameter measurement and simulation.

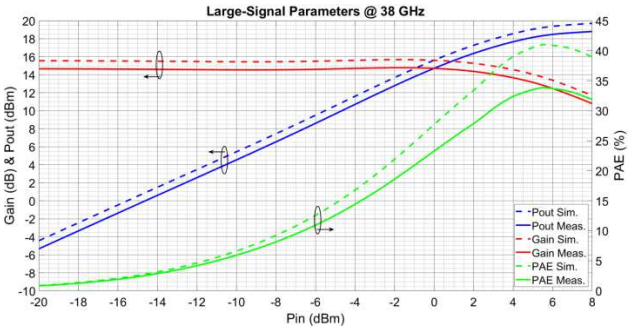

Fig. 10. Large-Signal Parameter measurement and simulation.

As for the large-signal measurement (Fig. 10), the proposed quasi-inverse class F PA exhibits a large-signal power gain $Gain > 14\ dB$ at the operating frequency of 38 GHz, as well as an output 1-dB compression point $OP_{1dB} \approx 17.6\ dBm$, a saturation delivered power $P_{sat} \approx 19\ dBm$ and a peak $PAE \approx 33\%$. Furthermore, looking into Figure 11, where the OP_{1dB} and PAE are plotted over the frequency range $37 - 40\ GHz$, it should be noticed that the designed PA performs high enough $OP_{1dB} > 16\ dBm$ and $PAE > 30\ \%$ for the whole band of interest. Other important specifications arising from our measurements are the $IIP_3 \approx 9\ dBm$ as well as the AM-to-PM conversion $< 20°$.

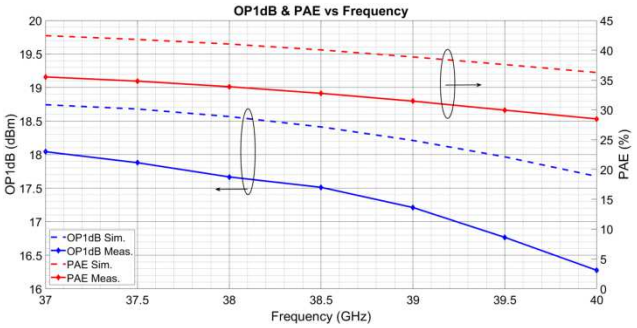

Fig. 11. Measurement and simulation results of OP1dB and PAE over frequency.

TABLE II
PERFORMANCE COMPARISON IN 130 NM SIGE PAS

Reference	[10]	[11]	[12]	This Work
Class/Stages	F^{-1} / 2	F^{-1} / 2	E / 2	Quasi-F^{-1} / 1
Freq. (GHz)	39-42	38	40	37-40
Gain (dB)	>15	22	15.4	>14
OP_{-1dB} (dBm)	>16	17.5	22.2	>16
PAE (%)	>40	30	20.8	>30

VI. CONCLUSION

This paper presents a 37-40 GHz, single-stage, quasi-inverse class F PA, integrated in a 130 nm SiGe BiCMOS process. The PA adopts a harmonically tuned load in order to provide the required impedances to the cascode amplifying core. Furthermore, this paper discusses the methodology for the accurate discovery of the active device's parasitic capacitance, a common problem in PA design. Moreover, a simplified model for the extraction of time-domain intrinsic voltage and current waveforms is introduced, enforcing the accurate characterization of the HBTs. Table II exhibits a short performance comparison in SiGe PAs that use harmonic tuning to their output stage for enhancing efficiency.

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