# Power Analysis Methodology for Energy Harvesting System on Chip

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***Abstract*— In this work, a novel power analysis methodology is proposed, aiming to successful simulation and accurate power drop analysis of fully integrated energy harvesting SoCs. The proposed methodology exploits the PySPICE open-source Python module and the NgSPICE open-source simulator, enabling full-chip rapid power analysis and large signal – transient results' extraction. A D-latch 9-stage ring oscillator scheme is implemented in a nanometer CMOS process, as the basic cell of the product vehicle. The cell emulates the power contribution of the energy harvesting system's digital block. Advanced power grid parasitics-aware simulations' results are presented, accompanied with the simulation performance metrics, to validate the power analysis methodology. The presented technique enables power simulation-aware package and PCB design.**

***Keywords—power integrity, voltage drop, PySPICE, NgSPICE, simulation speedup, large signal analysis, system on chip, energy harvesting***

## I. INTRODUCTION

The energy harvesting concept is widely used in every technological field, as a robust power supply solution [1]. A plethora of applications such as structural health monitoring, medical implantable sensors and battery charging for large systems, relies on renewable environmental sources for undisrupted, perpetual operation [2]. Synchronous energy harvesting systems are implemented in silicon, to enable small-sized, highly efficient solutions [3]. As the technology progresses, the energy harvesting systems become more sophisticated. Large digital blocks are utilized, to enable effective system control and high performance, substituting complex analog circuits (i.e., multipliers, sample and hold units, analog-to-digital converters) [4]. These standard logic cell blocks present high frequency switching, which greatly affect the power integrity of the chip, imposing major reliability issues and operation failure risk [5].

A chip's power supply is evenly distributed to the circuit blocks through the power delivery network (PDN). The PDN consists of metal lines and vias, providing the power path, from the positive voltage supply rail (VDD) to the circuit blocks [6]. Each metal line presents finite resistivity. As Ohm's law indicates, when current flows through the power grid, a voltage drop (also referred as IR drop) is observed. The value of the voltage drop ($\Delta V$) depends on the impedance of the network and the flowing current ($\Delta V = IR$). For large impedance and current values, the voltage drop may exceed the safety margins. In this case, the real supply voltage value of the logic gates will be significantly lower than the applied voltage. This can cause critical issues to the operation of the chip and also can decrease the application's reliability.

In particular, the decrease of the power supply affects the gate swing of the standard cells, leading to increased delay. This phenomenon interferes with the setup and hold timing of design. For this reason, certain paths of the power grid may become critical [7]. If the voltage drops below critical levels, the standard cells cannot operate, leading to functional failure of the chip. Furthermore, increased switching activity can induce power noise, i.e., voltage droops, in VDD rail and ground bounce in VSS. These instabilities in the supply nodes generate electromagnetic interference (EMI) issues, reducing the efficiency of the system [8]. Thus, optimum PDN implementation is a crucial step in the chip design process. The power distribution network should provide the chip's average power requirements, while ensuring safe operation and timing, during sudden switching phenomena.

With the semiconductors' scale down, the metal routings get narrower, layouts get more compact, and the switching frequencies progressively increase. The voltage drop problem becomes even bigger and the power integrity analysis prior fabrication is crucial [9]. Large energy harvesting ICs, comprising thousands of transistors, impose additional issues for the power integrity analysis execution. Due to the large netlist size, time domain simulations require impractical runtimes. In most cases, this leads to time consuming procedures, or even termination of the power analysis and incomplete design cycles [10]. Thus, the risk factor of operation failure and need for re-design critically increases.

To this end, a novel power analysis methodology is proposed, aiming to accurate simulation results and design cycle speedup. A Python-based chip power model is created, which effectively captures the switching current signatures generated by the standard cells (logic blocks) and the PDN parasitics. The full-chip power analysis is executed at early design stage (prior layout), enabling power drop-aware optimum package and PCB design. Python is selected as it presents high versatility, efficiency, and speed, while providing hundreds of libraries and frameworks. PySPICE open-source Python module is exploited to provide a Python interface to the NgSPICE circuit simulator. PySPICE offers a netlist-based definition of the circuit, simulation using NgSPICE, as well as analysis of the output using Numpy and Matplotlib. NgSPICE open-source simulator uses netlists and commands to run simulations, eliminating the need of overlaid GUIs. In addition, integration of SPICE simulator in Python leads to extreme adaptation capabilities [11].

Section II discusses the state-of-the-art power analysis methods; Section III presents the proposed design methodology and Section IV demonstrates the simulation results. Finally, Section V concludes this paper.

## II. STATE-OF-THE-ART POWER ANALYSIS METHODOLOGIES

Power integrity analysis and IR drop testing is a fundamental step in the chip design process. In 1999, Smith et al. presented for the first time, the concept of target

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impedance extraction in the frequency domain [12]. The analysis was based on the PDN impedance characteristics (resistance, capacitance, inductance) evaluation, aiming to the power supply noise minimization. Since then, power integrity analysis and optimum PDN design have been extensively studied and employed in the integrated circuits (IC) design flow.

Commercial electronic design automation (EDA) tools such as Ansys Redhawk-SC [13] and Cadence Voltus [14] have been developed, enabling power noise and reliability signoff for digital SoCs. These EDA tools generate vector-based chip power models or vector-less dynamic current profiles. These approaches are quite complex for large SoC implementations and require extremely long simulation times, which slows down the design cycle.

Many works propose numerical techniques, such as the finite difference time domain (FDTD) method [15][16] and the boundary element method [17], focusing on the PDN modeling. In these techniques the chip's geometry is parsed, and system equations are used to produce the chip's current or voltage signals at various power nodes. Scattering parameter analysis is adopted to produce these methods results. As these are black-box methodologies, the relationship between the frequency response and the on-chip current paths is quite difficult to determine.

The digital core logic is typically modeled with piecewise linear current sources, which are distributed all over the silicon die, as a function of the individual logic cells [18][19]. Although these methods enable highly accurate results regarding the SoC's power integrity simulation, they are extremely time consuming.

Recently, various works have been published, executing power integrity analysis via Neural Networks (NN) or machine learning (ML) algorithms [10][20]. Although these methods seem promising, they are case-dependent, meaning that they are dedicated to designs that have been included in the training dataset. Hence, a new algorithm must be created and trained for each distinct design, which defeats the purpose of a generic solution for power analysis speedup.

## III. Proposed Power Analysis Methodology

Fig. 1 depicts the chip power grid (VDD to VSS) and the core logic blocks connected between the power rails.

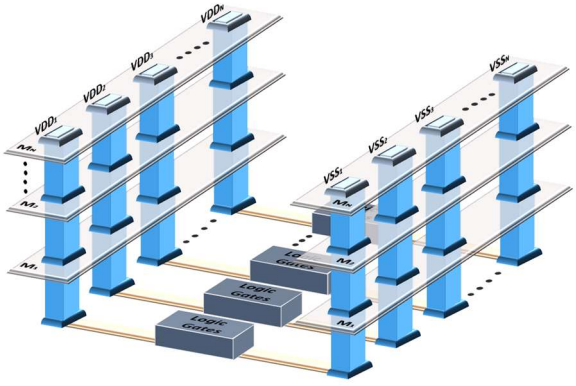



Fig.1. Chip power model concept.

A mesh-type PDN design is adopted, based on the technology's metal options. Metal stacks of Metal1 to Metal3 and Metal4 to Metal6 form the VDD and VSS power grids, respectively. Each core logic block is connected between $VDD_x$ and $VSS_x$ power nodes throughout the silicon die. Power is offered to the chip via the package and printed circuit board (PCB) power supply lines.

For the PDN impedance, in-between the power nodes, a SPICE model is adopted, depicted in Fig. 2. The equivalent circuit model consists of an inductor, a series resistance and two capacitors, to emulate the capacitive coupling to ground.

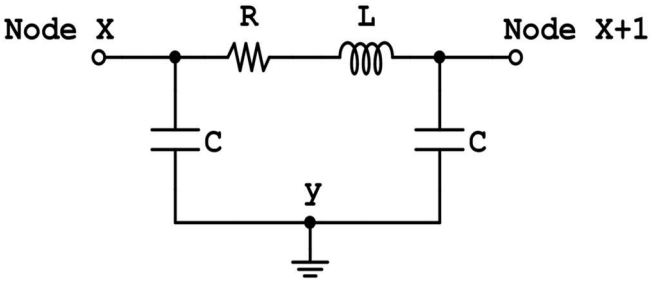



Fig.2. PDN impedance equivalent circuit model.

The most challenging part is the modeling of the chip's digital logic blocks. A Python framework is adopted, eliminating the need of SPECTRE simulations which impose prohibitively high complexity to the system's power analysis. The proposed methodology is an automated command-line procedure. The respective data and operations flow are depicted in Fig. 3.

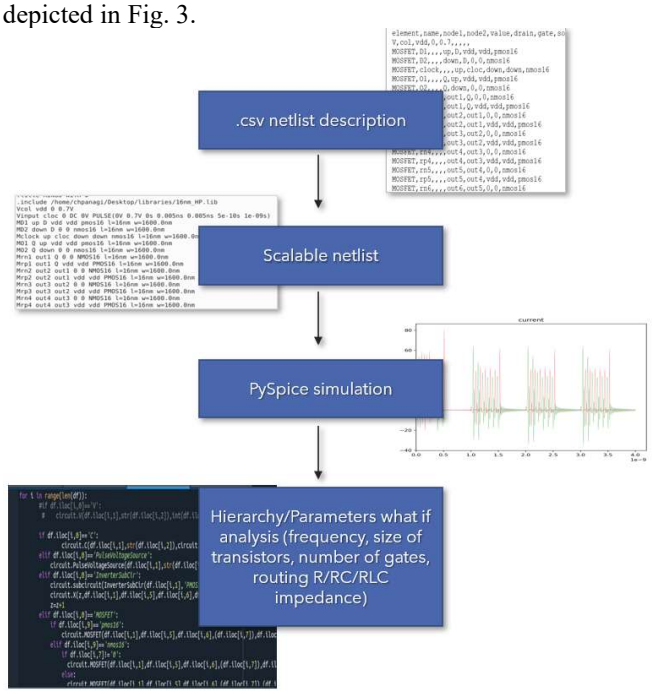



Fig.3. Proposed design methodology flowchart.

A Python source code script, in .csv format, translates all the cell's parameters and the full-blown digital architecture into a discrete Python-based netlist, suitable to be parsed with PySPICE. This produced netlist is scalable versus the design parameters and the full hierarchy, meaning that the cells described in the netlist are parametrizable and the hierarchy is controlled in source code level. Simulations are carried out via PySPICE open-source module and the core NgSPICE simulator engine, producing plots of the full-chip's voltage and current signature signals. A "what if" analysis is carried out by varying the used cell's parameters (e.g., frequency,

transistor sizing, number of gates, PDN R/RC/RCL impedance). The proposed design methodology enables auto-generation of .csv large scale (Mgates) netlists, full hierarchy definition and seamless scale up in the open-source Python interface. The full engine, from the .csv Mgates logic definition to the full-blown large signal simulation, is performed in Python source code level. "On the fly" adaptation of the network's parameter is provided. The exploitation of Python's computational power and capabilities for the IR drop testing leads to minimization of iterations and overall process speedup. At the same time, highly accurate time domain (transient) analysis results are extracted in the early design stage, including the PDN parasitics, having no available physical design. Hence, power drop-aware optimum package and PCB design is enabled.

## IV. Proposed Chip Power Model Validation

### A. D-latch ring oscillator basic cell IR drop Vehicle

A D-latch 9-stage ring oscillator is used as the basic cell of the digital logic block [21], to validate the chip power model and extract the method's performance metrics (Fig. 4). The circuit oscillates while the positive edge-triggered D-latch's output (Q) is high. A voltage pulse source provides clock synchronization to the delay latch, at 1 GHz frequency. To provide higher complexity to the basic cell, branches of inverters are connected between the ring oscillator's stages. The basic IR drop cell is composed of 100 gates.

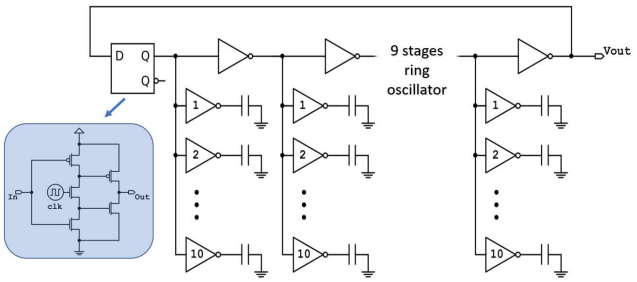



Fig.4. D-latch 9-stage ring oscillator basic IR drop cell.

A 22nm CMOS Process Design Kit (PDK) is selected for the implementation of the IR drop Logic Architecture. The width of the transistors is set to 1200 nm and the length of the transistors is set to 12 nm, both for PMOS and NMOS devices. The supply voltage (VDD) is 0.95 V. Fig. 5 depicts the operation of the basic IR drop cell.

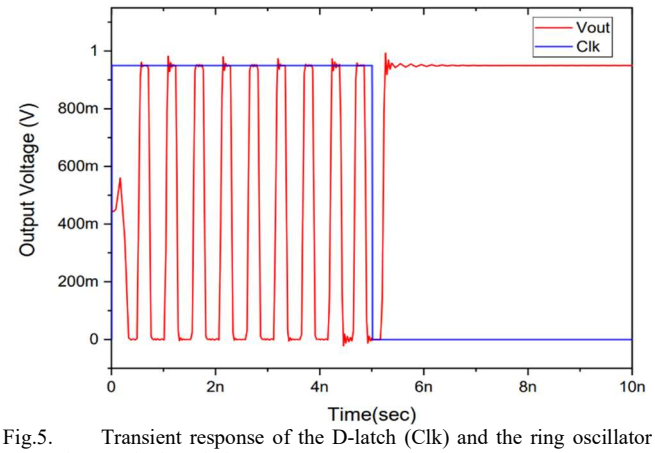



Fig.5. Transient response of the D-latch (Clk) and the ring oscillator (Vout) in one clock period.

When the D-latch (Clk) presents a high output, the ring oscillator circuit is activated, and oscillations are generated at the circuit's output (Vout). At the moment that the D-latch's output voltage drops to 0 V, the oscillations stop, and the ring oscillator circuit is deactivated.

Fig. 6 depicts the VDD current signature of the basic IR drop cell. When the ring oscillator circuit is ON, the switching activity of the standard cells cause extreme fluctuations in the current signal drawn from power rails.

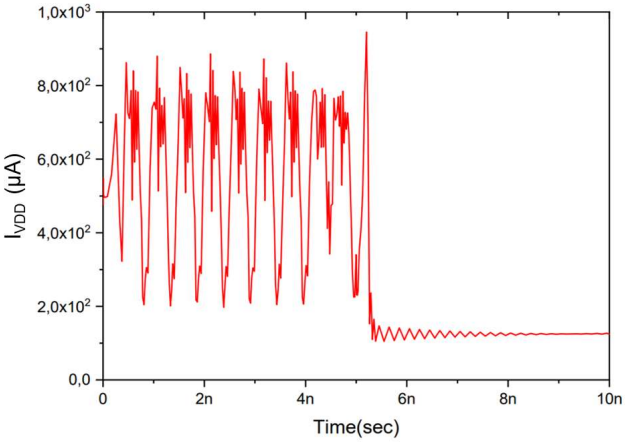



Fig.6. Basic IR drop cell's VDD current signature.

### B. Digital logic product vehicle

Fig. 7 presents the structure used for the proposed methodology validation. The model of Fig. 2 is used for the PDN network. The digital circuitry is a chain of logic blocks, identical to the basic cell of Fig. 4, distributed with a uniform way onto the power (VDD) and ground grid. In total, 10 families of gates (basic cells) are used, forming a kgate logic architecture. Each basic cell is connected to the digital VDD and VSS (y) power rails, providing $I_{VDD}$ switching currents. A logic cell power grid address ($x_1$, $x_2$,..,$x_n$) is assigned to each node. Thus, the switching currents of each gate family can be monitored and simulated separately. Vtest is a 0 V ideal voltage source, used as probe for the PySPICE simulator, to measure the desired signals. This way, the voltage and current signal variations during the switching operation can be captured.

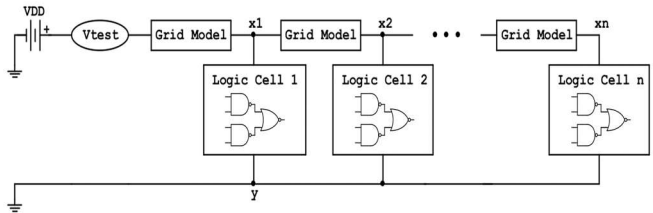
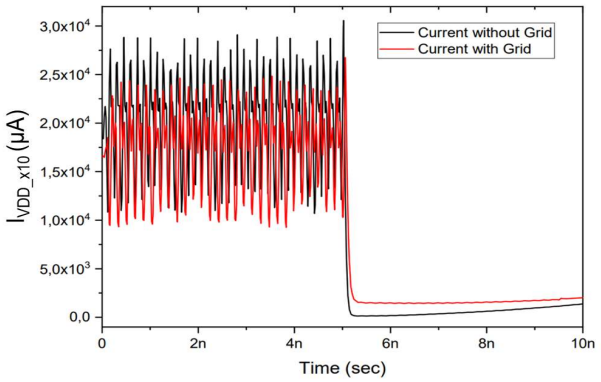



Fig.7. Power grid and logic model network.

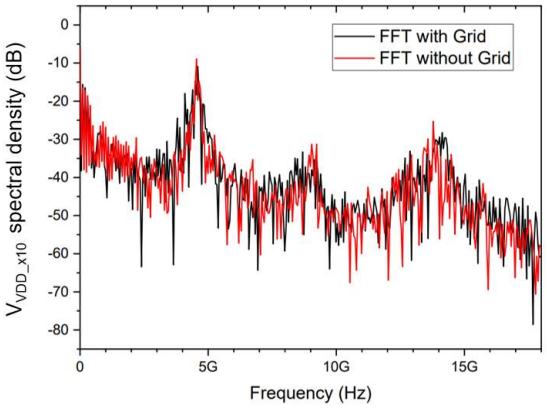
To validate the performance of the proposed chip power model, simulations of an ideal version of the power grid, where no parasitic RLC elements are present, are compared with an RL based PDN impedance model. In the latter case, the grounding capacitors' value is considered negligible. To extract realistic results, based on respective electromagnetic simulations, R is set to 100 mOhm and L is 0.1 fH.

Fig. 8(a) presents the current signals, measured at x10 node. The black signal corresponds to the ideal power grid and the red signal to the RL-aware impedance grid. As depicted, there is significant variation between the two power supply

currents signatures. The non-ideal grid's current spikes are smaller, due to the path's impedance. The simulation results are also extracted in a frequency response form. Fig. 8(b) presents the Fast Fourier Tranform (FFT) analysis of x10 node voltage signals for both cases. The peak current values in the frequency domain provide essential information for the PCB design and the decoupling capacitor selection, as to tune the respective package and PCB power rails impedance value outside the frequency region of our digital architecture. This information is only available if the PDN parasitics are included in the early phase simulations of the logic, and this is feasible based on the virtual scalable impedance model added in the Python based simulation framework.




(a)




(b)

Fig. 8. (a) x10 node current signals with ideal power grid and RL parasitics grid in the time domain. (b) FFT analysis of x10 node voltage signals.

For the RL-aware power grid, the switching current signatures of various nodes are depicted in Fig. 9. As expected, the IR drop increases in each stage, as the total power path impedance also increases.

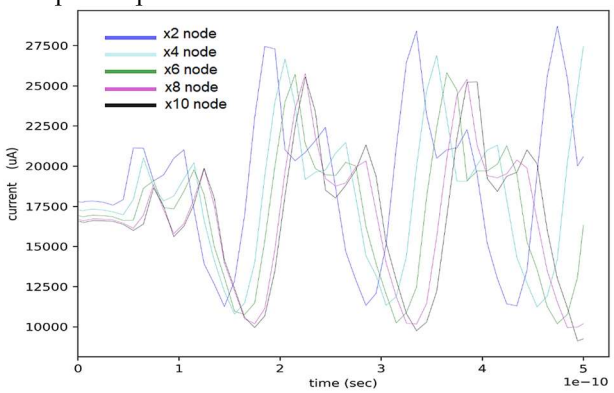



Fig. 9. Zoom-in switching current signatures of nodes x2, x4, x6, x8, x10 for the RL-aware power grid.

Fig. 10 presents the $I_{VDDx}$ (rms current) for the power grid nodes. As presented, the current drawn from the power supply progressively decreases, as voltage drop increases due to the power grid's RL parasitics.

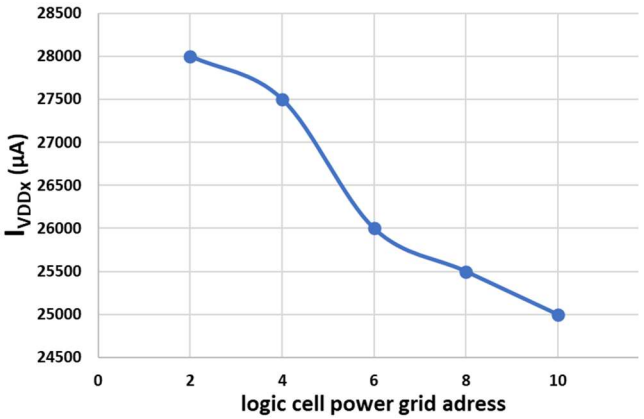



Fig 10. IR drop of power nodes x2, x4, x6, x8, x10 for the RL-aware power grid.

Table I presents the comparison of the proposed power analysis methodology with the standard large signal analysis. The PySPICE-NgSPICE based methodology requires 5 hours to provide the power analysis output results, while the standard simulation flow via Cadence SPECTRE simulator fails to complete the large signal analysis, due to the extremely large netlist size of the product vehicle. Furthermore, in the proposed technique, a .csv netlist format is adopted, which transforms all cell's parameters into discrete netlist values and provides "on the fly" adaptation of design parameters and the full hierarchy. Compared to the standard methodology, where the netlist consists of RLC components and BSIM models and scalability is not possible, the Python-based implementation enables extreme design cycle speedup, minimizing the number of design iterations. Furthermore, the proposed methodology is PDN parasitics-aware and is suitable for early design stage execution, while the standard analysis does not include the power grid's parasitics and requires post layout simulations, increasing the iterations between the schematic and layout and vice versa.

TABLE I. STANDARD VERSUS PROPOSED METHODOLOGY

| | **Standard methodology** | **Proposed methodology** |
|---|---|---|
| **Simulation time** | impractical | 5h |
| **Simulator** | SPECTRE/SPICE | PySPICE/NgSPICE |
| **Logic Description** | RLC & BSIM | .csv |
| **Scalability** | no | yes |
| **PDN parasitics** | no | yes |
| **Early Design IR drop simulation** | no | yes |

## V. CONCLUSIONS AND FUTURE WORK

In this work, a novel power analysis methodology for energy harvesting SoCs is proposed. Modeling of the SoC's digital logic, as well as the chip's PDN network is implemented, via a Python-based framework. Automated generation of large-scale netlists is achieved, while offering full hierarchy definition and seamless scale up. Furthermore, "on the fly" adaptation of the network's parameter is

provided. Python's computational power is exploited for minimization of the simulation runtime, enabling overall process speedup. More importantly, large signal analysis results are extracted in early design stage, avoiding chip operation failure and redesign. The proposed methodology is applied on digital circuitry grid, composed of ring oscillator-based gate families. The simulation results validate the effectiveness of the proposed design methodology. Large signal IR drop results are extracted, regarding the chip power model characteristics, leading to valid power drop estimation. Optimum PCB design and package selection can be enabled, based on the proposed power analysis methodology.

In future work, the presented chip power model simulation results, extracted from the Python based methodology, will be compared to IR drop measurements from the energy harvesting SoC's fabricated die. Furthermore, NgSPICE open-source code adaptation will be performed, aiming to large signal analysis speedup.

## ACKNOWLEDGEMENT

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