Design and Implementation of a D-Band I/Q Modulator in a 130 nm SiGe BiCMOS Technology

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***Abstract*—In this paper a D-Band direct conversion quadrature I/Q Modulator, integrated in a 130 nm SiGe BiCMOS process, is presented. The proposed design is based on double-balanced Gilbert-cell mixer and it is able to perform efficient up-conversion of wideband baseband signals, supporting gigabit communication in the D-Band. The modulator is broadband, in terms of the LO frequency range, maintaining a conversion gain higher than 5dB for various LO tones between 130-160 GHz. The circuit achieves a LO-to-RF isolation of 41 dB and an image rejection of 40 dB when it is driven with 0 dBm LO power. The power consumption of the proposed modulator is lower than 90 mW.**

Keywords—active mixer, I/Q Modulator, D-band, SiGe BiCMOS, conversion gain, gilbert cell, up-converter, quadrature double-balanced

I. Introduction

With the first steps of 5G technology, new ideas and innovative plans have already been formed for 6G technology. The 6G will introduce the new communications society of 2030 providing additional capabilities and technologies to serve user demands [1]. High data rate requirements push the communication systems to millimeter-wave frequency bands while organizations are exploring the innovative field of THz technologies. Several research results promise unlimited and full wireless communication in the near future, enforcing the capabilities of various applications such as radars, navigation, positioning, sensing, mobile communications, etc [2], [3]. Thus, the requirements for the new 6G networks relate to spectrum and power management, peak data rate, latency, capacity and mobility. More specifically, peak data rate is expected to exceed 1 Tb/s, i.e., 100 times higher than 5G, user-experienced data rate 1Gb/s, i.e., 10 times higher than 5G, latency 10-100 μs, 10 times higher network density than 5G, energy efficiency 10-100 and spectrum efficiency 5-10 times higher than 5G [4].

This paper deals with the design and implementation of an integrated D-Band quadrature I/Q modulator, one of the most critical blocks in modern mm-wave and sub-THz transmitters [5]. Implementations of D-Band I/Q modulators are included in several recent 6G and beyond 5G applications [6], [7], [8]. Such a circuit is responsible for the up-conversion and amplification of the baseband signal into the D-Band. The proposed design is based on the double-balanced Gilbert-cell mixer [9] and it is fully integrated in a 130 nm SiGe BiCMOS technology. The designed I/Q modulator is intended for becoming part of a D-Band transmitter, able to support gigabit short-medium range data links using Polymer Microwave Fibers (PMF). The design focuses on linearity, both in terms of frequency and input power, conversion gain and power consumption.

The paper is organized as follows: In section II, the transmitter's block diagram, in which the proposed design forms an irremovable part, the schematic and layout design of the I/Q modulator are discussed. In section III, the post-layout simulation results are presented.

II. Up-Conversion I/Q Modulator

A. Transmitter Blockchain

The quadrature I/Q modulator is designed to operate optimally in the specific transmitter blockchain shown in Fig.1. The broadband behavior of the modulator enables the gigabit baseband data translation into the D-Band.

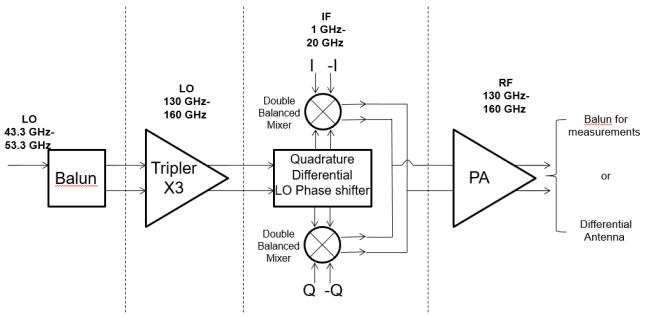

Fig.1. Transmitter block diagram for gigabit communication.

For this purpose, most of the specifications were selected regarding the transmitter's requirements. Input and output ports are differential, terminated at $100\ \Omega$, and the conversion gain should be high enough in order to reduce the requirements of the power amplifier that follows. To achieve this, an active topology of two gilbert-cells is selected for the modulator aiming for the minimum possible power consumption.

B. Mixer Design

The active mixer was designed in a double-balanced, Gilbert-cell topology as shown in Fig.2. All active devices are HBTs, with the same emitter mask width of $0.22\ \mu m$. The switching stage consists of two emitter-coupled pairs [10] Q1, Q2, Q3 and Q4, with emitter mask lengths equal to $2.7\ \mu m$,

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and they are biased near to pinch-off region, acting as switches. For the transconductance stage, transistors Q5 and Q6, with emitter lengths equal to 4.5 μm, convert the IF voltage signal to current and they are biased into the optimum current density for maximum ft [2]. Tail-current is flowing though the HBT Q7 which has an emitter mask length of 10 μm.

Transmission lines TL1 and TL2 are used for inductive emitter degeneration, improving the linearity of the mixer while the lines TL3, TL4 at the output, are used to enforce the achieved conversion gain [10]. In this technology, the 50-Ω transmission lines consist of top-metal strip, using wider intermediate-metal strip as a return path. On-chip matching networks comprised of MIM capacitors, transmission lines and TaN resistors are added at the LO, IF and RF ports to achieve the broadband frequency tuning. The mixer cell is under a 3.3 V supply voltage while the biasing of each HBT is performed with externally controlled independent voltage sources through polysilicon resistors.

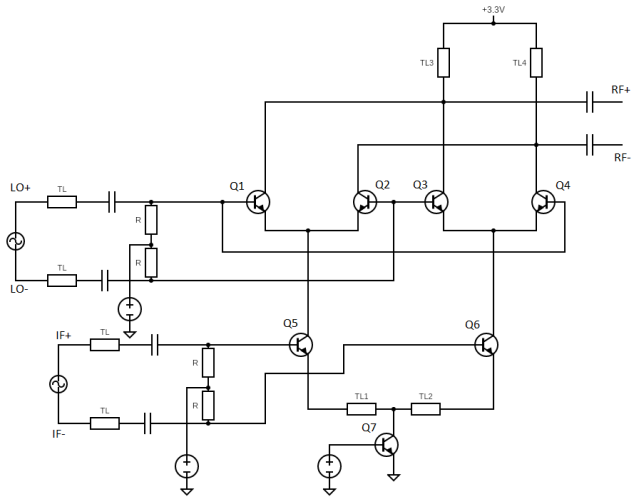

Fig.2. Schematic of the proposed D-Band mixer cell.

C. *Modulator Design*

The modulator consists of two up-converting mixer cells, with the same topology as shown in Fig. 2. The two mixers operate in quadrature, modulating the differential I and Q signals with the differential LO_I (0º phase) and LO_Q (90º phase) signals respectively [11]. In such a way, a remarkable image rejection ratio is achieved with no use of additional filtering [5]. The selected LO and IF signal phases are suitable for a lower sideband up-conversion operation (Fig. 3).

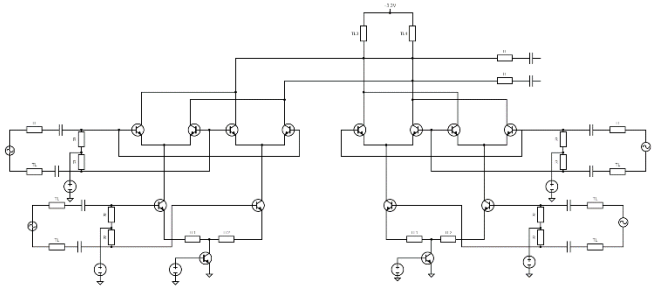

Fig. 3. Schematic of the proposed lower sideband up-conversion modulator.

D. *Layout Implementation*

The I/Q modulator is implemented in a 130 nm SiGe BiCMOS process with a transit frequency f_T of 250 GHz and an oscillation frequency f_{max} of 370 GHz. The technology features 6 copper layers and a top aluminum metal layer. MIM capacitors, polysilicon and TaN resistors are also available. The intermediate Metal 4 is used as reference ground, while Metal 3 is used as a power supply plane. Lower metals 1, 2 are used for dc interconnects. Low loss thick top metals 5 and 6 realize all the RF structures offering reduced capacitive coupling to the ground.

In order to provide the proper LO phases at the bases of the HBTs of the switching stage, a well-defined differential LO coupler is inserted between the LO generation circuitry and the modulator. Finally, the layout was implemented with the Cadence Layout tool and the final design is illustrated in fig. 4.

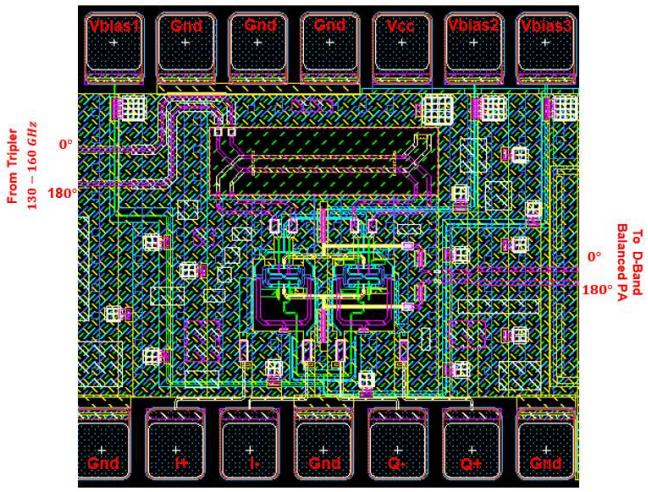

Fig. 4. Final layout of the proposed I/Q Modulator.

III. Simulation Results

The high frequency operation of the proposed I/Q modulator requires an accurate modeling of transistors' metal interconnects. Thus, RC parasitic extraction up to metal 4 is used for all the selected HBTs while the interconnect up to top metal 6 as well as all the RF structures and matching networks are EM simulated via Momentum ADS.

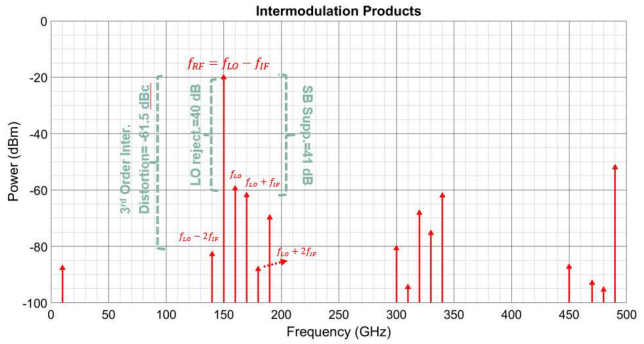

Fig. 5. Output spectrum for a LSB Up-Conversion.

Fig. 5 shows the output spectrum for $f_{LO} = 160\ GHz$, $P_{LO} = 0\ dBm$, $f_{IF} = 10\ GHz$, $P_{IF} = -25\ dBm$. A 40 dB

LO rejection ratio and a 41 dB image suppression are accomplished for such a simulation scenario.

Fig. 6 shows the conversion gain versus the IF frequency for various LO frequencies having set the LO and IF power level to 0 dBm and -30 dBm respectively. The results show that the proposed design is able to maintain an almost flat conversion gain higher than 5 dB for wide IF frequency range.

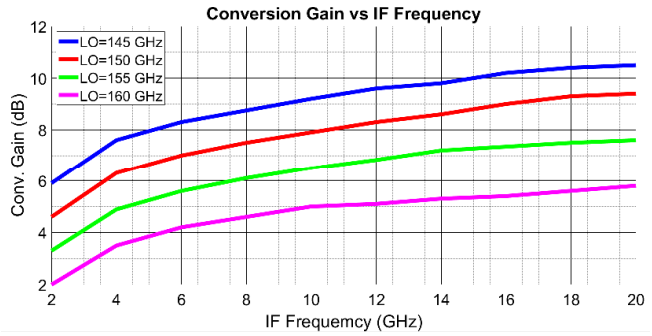

Fig. 6. Conversion gain over IF frequency for various LO tones.

Moreover, the conversion gain versus IF and LO power for $f_{IF} = 5\ GHz$, $f_{LO} = 150\ GHz$, is presented in fig. 7 and 8 respectively. As it shown the modulator achieves a conversion gain higher than 6 dB for IF input powers up to -20 dBm. Also, fig. 8 denote that LO power can boost the conversion gain up to a value in which further LO power increase does not correspond to further increase of the conversion gain due to mixer's compression.

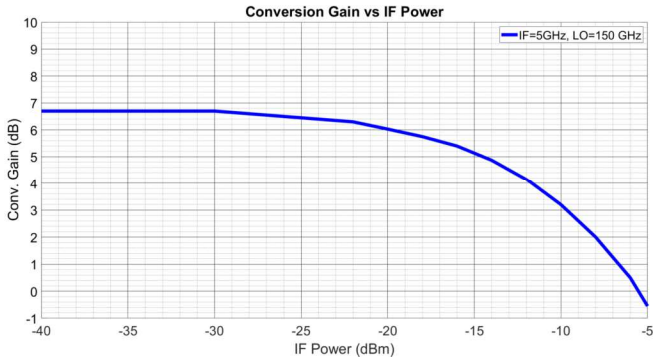

Fig. 7. SSB conversion gain versus IF power for $f_{IF} = 5\ GHz$ and $f_{LO} = 150\ GHz$.

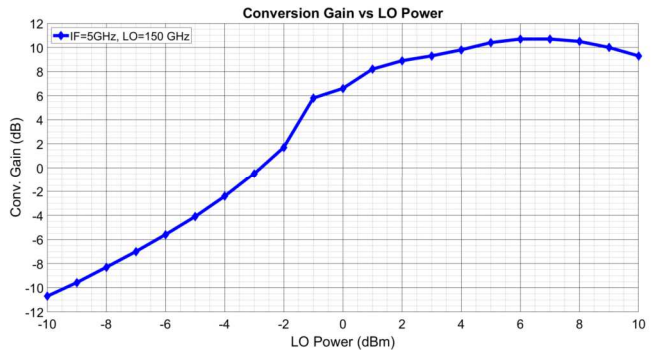

Fig. 8. Conversion gain versus LO power for $f_{IF} = 5\ GHz$ and $f_{LO} = 150\ GHz$.

The output power versus input IF power for $f_{IF} = 10\ GHz$ and $f_{LO} = 160\ GHz$ is illustrated in Fig. 9. The IP1dB is around -15 dBm and the OP1dB is -11 dBm, for LO power equal to 0 dBm.

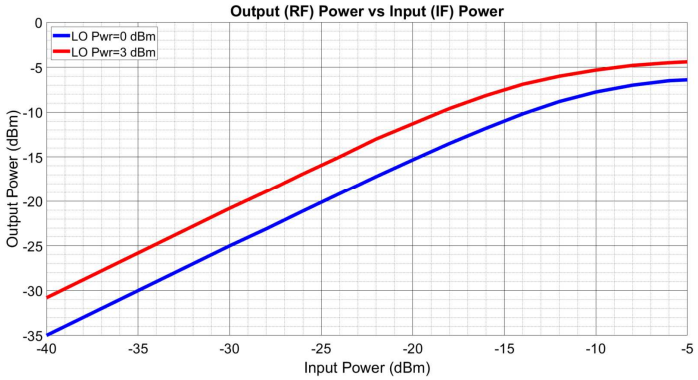

Fig. 9. Output power versus IF power for $f_{IF} = 10\ GHz$ and $f_{LO} = 160\ GHz$.

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A graph representation of the LO leakage over the LO frequency range for two different LO power levels is illustrated in Fig. 10. In both cases the LO rejection ratio is higher than 35 dB for the entire LO frequency range. Also, it is clearly denoted that for lower LO power levels the LO rejection ratio maintains higher values.

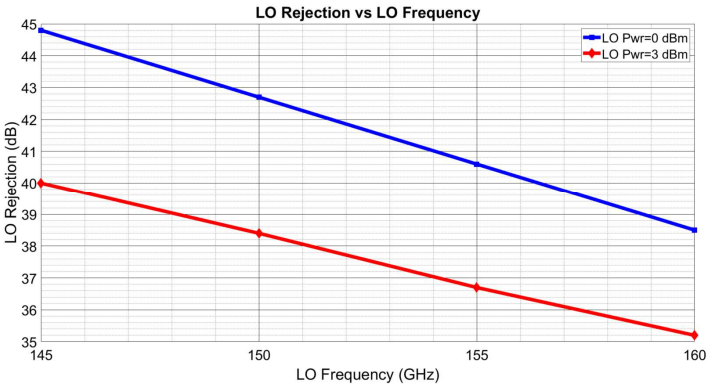

Fig. 10. LO rejection over LO frequency when $f_{IF} = 5\ GHz$, $P_{IF} = -25\ dBm$.

Moreover, the sideband suppression versus the LO frequency is represented in Fig. 11, similarly, for two different LO power levels. In both cases the sideband suppression is higher than 38 dB.

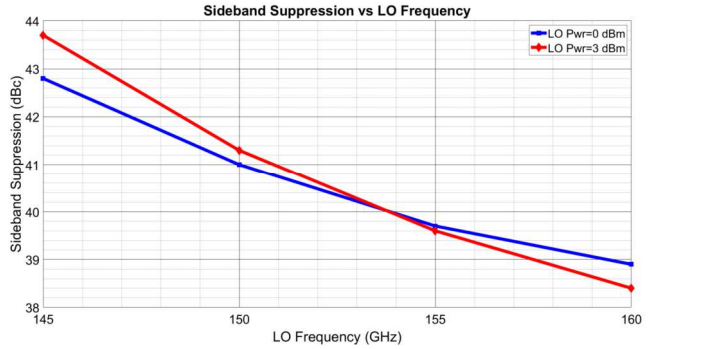

Fig. 11. Sideband Suppression over LO frequency when $f_{IF} = 5\ GHz$, $P_{IF} = -25\ dBm$.

Finally, the scattering parameters of the input and output ports are depicted in Fig. 12. The small-signal simulation results show that the LO and RF ports are well-matched to the differential $100\ \Omega$ load while the matching at the IF port is almost flat for the frequency band of interest.

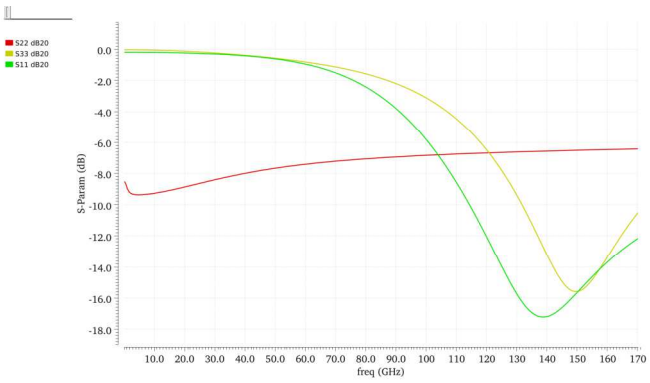

Fig. 12. Small-signa s-parameter simulation. S11 stands for LO input, S22 for IF input and S33 for RF output.

In order to test the phase mismatches in both IQ and LO ports we run two more simulations with a small rotation of 2 degrees in both differential ports. The results for the conversion gain and the LO leakage show negligible changes from the initial results, less than 0.3dBc.

Additionally, Process, Voltage and Temperature simulation were realized, to verify proper operation in all possible conditions. Running a Monte Carlo simulation, we get low standard deviation (sd~1) in all cases for the process variation test. Also, the results show a maximum fluctuation of the output power of 1dBm for a ±30% voltage supply sweep and of 20dBm for a temperature sweep from -10ºC to 100ºC.

A performance comparison between the proposed design and the state-of-the-art I/Q modulators is provided in Table I. It should be noted that the performance of the current work is related to simulation results.

TABLE I
COMPARISON TABLE OF PUBLISHED D-BAND I/Q MODULATORS

Ref.	Process	Freq.	Conv. Gain (dB)	LO-RF (dB)	RF/IF BW (GHz)	P_{dc} (mW)
This work	130 nm SiGe BiCMOS	120-160	>5	>35	40/20	90
[6]	250 nm SiGe BiCMOS	150-168	34	-	-	610
[12]	130 nm SiGe BiCMOS	119-152	9.8	31	33/13	53
[13]	65 nm CMOS	144	9.7	-	3.3/	219

IV. CONCLUSION

This paper presents a D-Band Quadrature I/Q Modulator. The design is based on double-balanced Gilbert cells and it is suitable for D-Band transmitters intended for gigabit communication. Simulation results denote that the proposed modulator is able to translate efficiently, up to $20\ GHz$ bandwidth baseband signal into the frequency range $120 - 160\ GHz$. The power consumption is quite low while the LO-to-RF isolation is remarkably high enforcing the performance of the whole transmitter.

REFERENCES

[1] W. H. Lin et. al., ”1024-QAM High Image Rejection E-Band Sub-Harmonic IQ Modulator and Transmitter in 65-nm CMOS Process,” IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 11, pp. 3974-3985, Nov. 2013.

[2] D. Parveg, M. Varonen, M. Kärkkäinen, D. Karaca, A. Vahdati, and K. A. I. Halonen, “Wideband millimeter-wave active and passive mixers in 28 nm bulk CMOS technology,” Proceedings of the 10th European Microwave Integrated Circuits Conference, Paris, France, Sept 2015.

[3] P. de Maagt, P. H. Bolivar, and C. Mann, “Terahertz science, engineering and systems—From space to earth applications,” in Encyclopedia of RF and Microwave Engineering, K. Chang, Ed. New York: Wiley, 2005, pp. 5175–5194. K. Elissa, “Title of paper if known,” unpublished.

[4] K. David and H. Berndt, “6G vision and requirements: Is there any need for beyond 5G?” IEEE Veh. Technol. Mag., vol. 13, no. 3, pp. 72–80, Sept. 2018. doi: 10.1109/MVT.2018.2848498.

[5] S. Voinigescu, “High-frequency devices,” in *High-Frequency Integrated Circuits*, Cambridge, U.K.: Cambridge University Press, 2013, pp. 335-336.

[6] Y. Zhao, E. Ojefors, K. Aufinger, T. F. Meister and U. R. Pfeiffer, "A 160-GHz Subharmonic Transmitter and Receiver Chipset in an SiGe HBT Technology," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 10, pp. 3286-3299, Oct. 2012, doi: 10.1109/TMTT.2012.2209450.

[7] E. Laskin, P. Chevalier, A. Chantre, B. Sautreuil and S. P. Voinigescu, "165-GHz Transceiver in SiGe Technology," in *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1087-1100, May 2008, doi: 10.1109/JSSC.2008.920336.

[8] H. Yu *et al*., "High-Linearity Double-Balanced Up-Conversion Mixer with an Active Balun Based on InGaP/GaAs HBT Technique," *2018 International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, 2018, pp. 1-3, doi: 10.1109/ICMMT.2018.8563579.

[9] R. Svitek and S. Raman, “A SiGe active sub-harmonic front-end for 5–6 GHz direct conversion receiver applications,” in IEEE Radio Freq. Integr. Circuits Symp., Jun. 2004, pp. 675–678.

[10] Donald O. Pederson and Kartikeya Mayaram, “Analog Integrated Circuits for Communication”, Springer, 2008.

[11] K. Schmalz, W. W. J. Borngräber, W. Debski, B. Heinemann, and J. C. Scheytt, “A subharmonic receiver in SiGe technology for 122 GHz sensor applications,” IEEE J. Solid-State Circuits, vol. 45, no. 9, pp. 1644–1656, Sep. 2010.

[12] S. Carpenter, Z. S. He, and H. Zirath, “Multi-functional D-band I/Q modulator/demodulator MMICs in SiGe BiCMOS technology,” International Journal of Microwave and Wireless Technologies, vol. 10, no. 5-6, pp. 596–604, 2018.

[13] Tang A, Virbila G, Murphy D, Hsiao F, Wang YH, Gu QJ, Xu Z, Wu Y, Zhu M and Chang MCF (2012) A 144 GHz 0.76 cm-resolution sub-carrier SAR phase radar for 3D imaging in 65 nm CMOS, IEEE International Solid-State Circuits Conference, San Francisco, CA.