Charge-based time registers for z^{-1} implementation

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***Abstract*—Time-mode signal processing is an advantageous approach in which the time is the processing variable. Time register is used in the construction of time-mode z^{-1} operator which is the basic building block in the time-mode circuits and systems such as FIR/IIR filters and time amplifiers implementations. In this work, a comparison study between z^{-1} operators using different types of time register circuit is presented. The circuits of time-registers and z^{-1} operators are implemented in TSMC 65nm and are verified through simulations in relation to absolute error, signal-to-distortion ratio and current consumption.**

Keywords—Time-mode signal processing, time registers, z^{-1} operators, CMOS.

I. INTRODUCTION

The design of low-power analog circuits is becoming continuously challenging due to the device scaling, reduction of voltage headroom, power consumption minimization and necessity for higher resolution. Time-mode circuits are good candidates for replacing the conventional design approaches such as voltage-mode and current-mode circuits because of their better resolution, low power consumption and independency from device and voltage supply shrinking. The distinction of time-mode systems is that the information of interest is the time rather than the voltage or current as it is in the conventional equivalents [1].

In Fig. 1 the operation of a time-mode system is illustrated. Firstly, the information from voltage-mode (V_{in}) is converted into the time-mode (T_{in}) via a voltage-to-time converter (VTC). The sample-and-hold circuit samples, with a sampling period T_{sample}, the continuous voltage signal and then a pulse-width modulator converts the information into the time-domain. The magnitude of the time-mode information can be represented either as different values of pulse widths or as time intervals between pulse edges [2]. After the conversion, the information is being processed in the time mode. Finally, the time-to-voltage (TVC) converter reconstructs the time-mode processed information (T_{out}) into the corresponding output voltage signal (V_{out}). In many cases, TVC is replaced by a time-to-digital converter (TDC) for further processing by digital processors.

One of the most important building blocks of time-mode systems is the circuit of time register. The main goal of a time register is to store information on time-mode and recover it when it needed. The state-of-the-art time register architectures are separated into two basic categories: the charged-based time registers [3], [4] and the gate-delay based [5]. These circuits can be used as basic building blocks of more complex systems such as time-amplifiers [6], time adders/subtractors, time integrators [7] and time-to-digital converters [8].

Time registers can also be used in construction of z^{-1} operators. The main duty of a time-mode z^{-1} operator is to generate an output pulse with magnitude equal to its' input pulse, shifted over a period of the sampling frequency [9].

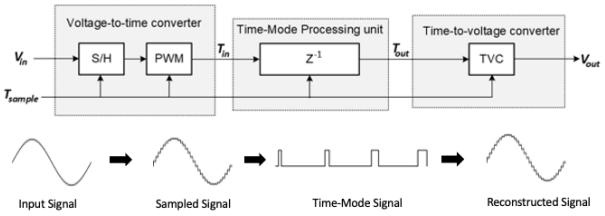

Fig. 1. Intuitevly time-mode processing system

This work presents and compare different types of charge-based time register. The comparison of time registers is taking place under a z^{-1} implementation, in respect to their absolute input-output time error, signal-to-distortion ratio and power consumption. The novelty of the work is that the z^{-1} implementation uses only two cascaded time registers compared with the z^{-1} implementations which use four cascaded time registers. In this manner the proposed z^{-1} operator occupies less area and consumes less power. Also, for first time in the literature the time registers are investigated in relation to the input-output time error and harmonic distortion.

The paper is organized as it follows. In section II the operation principle of charge-based time registers is presented as well as the architectures of the types of time register. Section III illustrates the z^{-1} operator architecture with time registers as building blocks. Section IV represents a performance comparison between z^{-1} operators which use different types of time registers. Finally, the conclusions from this comparison are presented in section V

II. CHARGE-BASED TIME REGISTERS

A. Time register with source-controlled discharging transistor (conventional)

Operation principle: The topology of the conventional charge-based time register is presented in Fig. 2(a) while the timing diagram is presented in Fig. 2(b). The *SET* is a digital signal; it is used to set the capacitor voltage to supply voltage V_{DD} when *SET*=0 ('0' means zero voltage). The input signal which is denoted as IN_{reg} is a voltage pulse train with pulse width equal to $T_{in.reg}$. The *CLK* signal is a digital signal with a pulse width (when *CLK*=1) equal to T_{CLK}.

It is assumed that a linear voltage-to-time converter is used as a front-end to convert the input voltage to a pulse train (with fixed frequency) in which the pulse width T_{in} is proportional to the input voltage [10], [11].

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Transistor M_2 acts as switch which is controlled by the output of OR gate. When M_2 is ON then the source of transistor M_3 is grounded and the discharging current I_{dis} is equal to the drain current I_{D3} of M_3 (I_{dis} =I_{D3}) which acts as current source. In case M_2 is OFF then the source of M_3 is floating and the discharging current becomes zero. Therefore, this type of time register is controlled through the source voltage of M_2.

When *SET*=1 ('1' means voltage equal to V_{DD}) and during the interval in which *IN*=1, the capacitor voltage V_{cap} is discharged with constant slope towards ground. When *IN*=0 then V_{cap} stays constant. When *CLK*=1 then V_{cap} is discharged again with the same slope. At the time when V_{cap} crosses the CMOS inverter triple point the output signal OUT_{reg} is asserted to V_{DD}.

Discharging slope: Assuming that M_2 is ON, the on resistance R_{ON2} of M_2 is sufficient small. So, the source of M_3 becomes zero and the current that discharges capacitor *C* is equal to the drain current I_{D3} of M_3. Also, the bias voltage *CTRL* and the aspect ratio of M_3 define the value of I_{D3}. Therefore, the discharging slope will be given by

$$slp = \frac{I_{dis}}{C} \tag{1}$$

Input range: Let's assume the case of input pulse width equal to zero, T_{in}=0. In this case, for the correct functionality of the time register, the capacitor voltage V_{cap} should be discharged from V_{DD} to the triple point of the inverter in a time interval equal to T_{CLK}. Therefore, the minimum slope should fulfill the next equation:

$$slp_{min} = \frac{V_{DD}-V_{tp}}{T_{CLK}} \tag{2}$$

Also, in case in which the maximum input pulse width $T_{in.reg.max}$ is applied, the capacitor voltage V_{cap} should be at least discharged to V_{tp} during a maximum input pulse width $T_{in.reg.max}$. Therefore, $T_{in.reg.max}$ should be equal to

$$T_{in.reg.max} = \frac{V_{DD}-V_{tp}}{slp_{min}} \tag{3}$$

which means that for achieving the maximum allowable input pulse width range, a spl=slp_{min} should be used. Based on eq.(2) and eq.(3) we take

$$T_{in.reg.max} = T_{CLK} \tag{4}$$

Output pulse width: Let's assume that an input pulse width $T_{in.reg}$ ($\leq T_{in.reg.max}$) is applied. The next equation will be always valid

$$V_{DD} - slp * T_{in.reg} - slp \cdot T_{out.reg} = V_{tp} \tag{5}$$

Also, it is valid that

$$V_{DD} - slp * T_{CLK} = V_{tp} \tag{6}$$

Therefore, combining eq.(5) and eq.(6) the output pulse width will be given by

$$T_{out.reg} = T_{CLK} - T_{in.reg} \tag{7}$$

achieving in this manner the registration of the value of $T_{in.}$

Registration input-output time error: The main causes of registration input-output time error $\tau_{er.reg}$ are a) the clock feedthrough due to fast transients appear at the gates of transistors M_1, M_2 and M_3 causes a voltage overshoot or undershoot $\Delta V_{cap.}$ on the V_{cap} b) the leakage current I_{leak} and c) the variation discharging slope Δslp due to the limited output resistance of current source transistor M_3. The error $\tau_{er.reg}$ is defined as

$$\tau_{er.reg} = T_{out.reg} - T_{out.reg.ideal} \tag{8}$$

where $T_{out.reg.ideal}$ is the output pulse width with no errors.

As long as the duration of ΔV_{cap} is small compared to $T_{in.reg}$ and T_{CLK} then the registration error is kept small. Without leakage current, voltage V_{cap} should be stay constant in case both T_{in}=0 and T_{CLK}=0. In reality, the leakage current discharges voltage V_{cap}, causing in this manner a time registration error. Finally, any variation of the discharging slope is translated into time registration error and harmonic distortion. Based on the above assumptions τ_{er} will be expressed intuitively by the next equation

$$\tau_{er.reg} = \tau_{er}(\Delta V_{cap}) + \tau_{er}(I_{leak}) + \tau_{er}(\Delta slp) \tag{9}$$

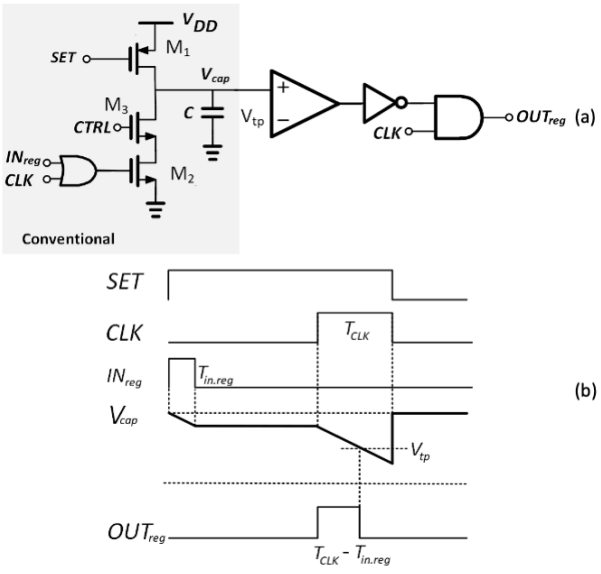

Fig. 2. a) Time register with source-controlled discharging transistor (conventional) and b) timing diagram

B. *Time register with drain-controlled discharging transistor*

The second type of time register is presented in Fig. 3. It is assumed that the functionality and timing diagram are the same for all types of time register. In the second type, transistor M_2 acts as switch disconnecting V_{cap} from the drain of transistor M_3. In this type, transistor M_3 acts as current source and its drain current I_{D3} is equal to the discharging current.

The advantage of this procedure over the conventional approach is that the current from the current source can be defined better because the source of the transistor that acts as current source is connected to the ground.

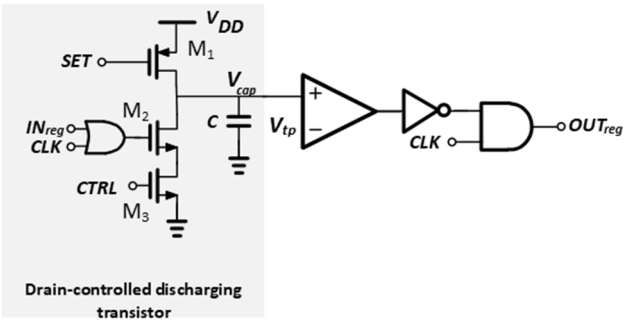

Fig. 3. Time register with drain-controlled discharing transistor

C. *Time register with gate-controlled discharging transistor*

The time register which is illustrated in Fig. 4 is the third type. The discharging current is the drain current I_{D3} of current source transistor M_3. There is no need for transistor between discharging transistor M_3 and capacitor node. The output of OR gate denoted as TR_{in} controls the gate voltage V_x of discharging transistor through appropriate switches. When TR_{in}=1, V_x becomes equal to *CTRL* and the discharging current is equal to I_{D3}. In case TR_{in}=0 then V_x becomes zero and the discharging current becomes zero. The switches presented in Fig. 4 are constructed by nMOS transistors.

The absence of a switching transistor that handles the behavior of the output capacitor, as it happens in the conventional approach is expected to lead in smaller clock feedthrough phenomena at the switching states of the circuit, because there is no node that is connected to the output which is forced in fast voltage transitions. On the other hand, the node between the source of transistor M_3 and drain of transistor M_2 in the conventional architecture is experiencing fast voltage changes when transistor M_2 transits from state OFF to state ON, leading to important clock feedthrough phenomena.

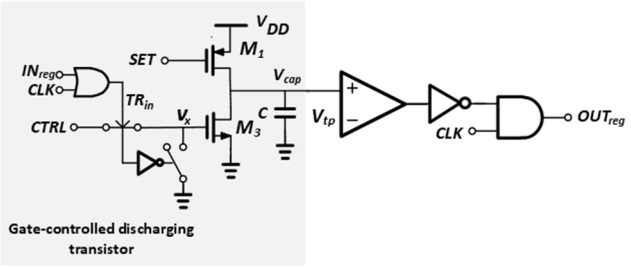

Fig. 4. Time register with gate-controlled discharging transistor

D. *Pseudo-differential time register*

The fourth type of time register is presented in Fig. 5. Transistors M_2 and M_3 have the same function as on the time register topology with drain-controlled discharging transistor. Transistor M_4 acts as a switch and its role is to pre-charge node V_x to V_{DD} when V_{cap} is disconnected (M_2 is OFF) from the current source transistor M_3.

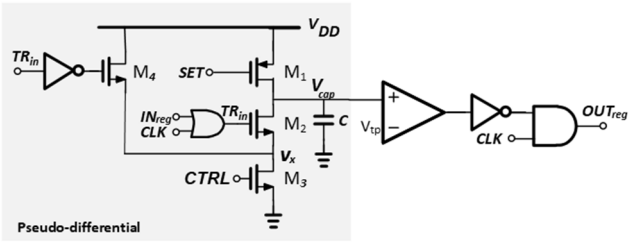

Fig. 5. Pseudo-differential time register

This modification is expected to face smaller clock feedthrough phenomena than the conventional type due to pre-charging node V_x from transistor M_4. When the transistor M_2 transits from state OFF to state ON, there is no voltage swing on the node V_x because it is pre-charged by transistor M_4. As a result, this behavior is eliminating the phenomena of clock feedthrough and the associated error $\tau_{er}(\Delta V_{cap})$, in contrast with the conventional approach which clock feedthrough phenomena have discussed in the previous topology.

III. Calibration of Time Register Slope

The discharging slope as it is given by eq.(1) depends on process and temperature variations of discharging current I_{dis} and capacitor C. The impact of these variation on the slope can be calibrated using analog or digital calibration negative loops [3], [9]. The calibration technique of these loops uses a reference input pulse width controlling the discharging current and producing an output pulse width until output and reference pulse width become almost equal no matters the process and temperature corners. The final calibrated slope features an error less than 20ps for a full-scale input pulse width of 40ns [9].

IV. z^{-1} Operators Based On Two Time Registers

A. *z^{-1} operation*

In Fig. 6 is illustrated the z^{-1} operator which consists of two cascaded time registers. Every time register contributes with a $z^{-0.5}$ operation on their input signal, resulting a z^{-1} operation between the input and the output of the circuit.

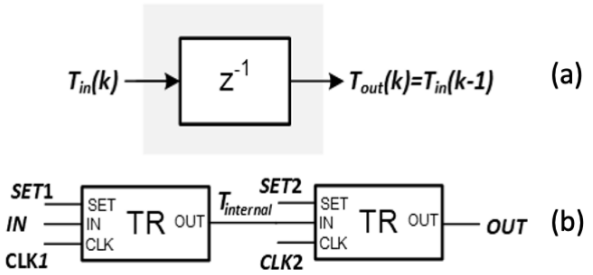

Fig. 6. (a) z^{-1} operator symbol and (b) z^{-1} topology

The timing diagram is represented in Fig. 7. The signals *SET*1 and *SET*2 have the same frequency, the same pulse widths but they present phase difference equal to a half of a period. Similarly, the signal *CLK*1 and *CLK*2 have also identical pulse widths with phase difference a half of a period. When *SET*1=1 the operation of the 1st time register leads to a pulse width $T_{internal}$ after half a period of *SET*1. The pulse width $T_{internal}$ is equal to:

$$T_{internal} = T_{CLK} - T_{in} \quad (10)$$

When *SET*2=1 the capacitor of the 2nd time register is discharged during the time intervals of $T_{internal}$ and *CLK*2, resulting to a signal in its output after a period of *SET*1 with pulse width equals to:

$$T_{out} = T_{CLK} - T_{internal} = T_{in} \quad (11)$$

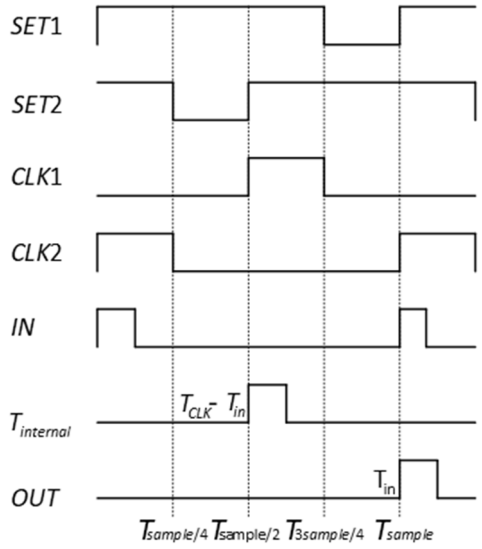

Fig. 7. Timing diagram of the z^{-1} operator

B. Absolute error of z^{-1} operator

The absolute error is referred as the time registration error between the input and the output of the z^{-1} operator. As we mentioned earlier every time register suffers from the time registration error τ_{er}, so the real values of the outputs of time registers that constitutes the z^{-1} operator are:

$$T_{internal} = T_{CLK} - T_{in} + \tau_{er.reg1} \quad (12)$$

$$T_{out} = T_{in} + \tau_{er.reg2} - \tau_{er.reg1} \quad (13)$$

Therefore, the absolute error τ_{er} of z^{-1} operator will be equal to

$$\tau_{er} = \tau_{er.reg2} - \tau_{er.reg1} \quad (14)$$

The time registers that constitute the z^{-1} operator are sharing almost the same time registration error that comes from clock feedthrough and slope variation phenomena. In contrast, $t_{er.reg}$ due to current leakage differs on each time register because it is dependent on the magnitude of time registers' input pulses T_{in} and $T_{internal}$, which have different pulse widths. As a result, in respect to eq.(14), only the time registers' registration error due to current leakage will contribute to the absolute error of the z^{-1} operator.

V. Simulation Results

The types of time register that are mentioned above are simulated under a z^{-1} implementation. The sampling rate was set at 5MHz. The circuits were designed in TSMC 65nm technology process and they were simulated using the Cadence Spectre simulator. The supply voltage was V_{DD}=1.2V. The CLK pulse width was T_{CLK}=50ns. The device sizes of all types of time register are presented in TABLE I.

The sizes of M_1, M_2 and M_4 transistors were selected to have small gate capacitance and low on resistance and hence, fast switching response and low leakage current to achieve small time registration errors. Size of M_3 was selected to have large gate-to-source resistance in order to function as a current source offering constant current and therefore accurate discharge slope.

TABLE I. Device Sizes W/L

M_1	M_2	M_3	M_4
130n/65n	130n/65n	3u/3u	130n/65n

In Fig. 8 is presented the block diagram of the testbench that was used for the performance measurements of the z^{-1} operator. It is consisted of a VTC which converts the input voltage signal V_{in} into a pulse train with pulse width T_{in}, the device under test (z^{-1} operator) and a TVC to convert it back on the voltage-mode V_{out}. The VTC and TVC are ideal components in order to not affect the measurements of z^{-1} operator. On the input of the system a sinusoidal voltage signal V_{in}=$0.5V_{DD}$+$V_{in.peak}$·sin(2πf_{in}·t) is applied, where $0.5V_{DD}$ is the average voltage, $V_{in.peak}$ is the amplitude and f_{in} is the input frequency. According to eq.(4), $T_{in.max}$=T_{CLK}=50ns, the pulse width of the converted signal will be:

$$T_{in}(t) = 25ns + T_{in.peak} sin(2\pi f_{in} t) \quad (15)$$

which means that T_{in} ranges between 0 and 50ns with sinusoidal manner and the maximum $T_{in.peak}$ is equal to 25ns.

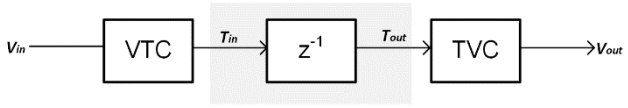

Fig. 8. Testbench for the perfomance measuring of z^{-1} operator

A. Abolute error of z^{-1} processing

The absolute error of the z^{-1} operator was measured via the difference in pulse width magnitude between T_{in} and T_{out}, using the testbench that was demonstrated in Fig. 8.

In Fig. 9 is presented the absolute time registration error τ_{er} over the entire range of T_{in}. Every type of time register has a specific region of input range in which they achieve a relatively small τ_{er}. This behavior is due to $\tau_{er.reg}$ of the individuals time registers that constitute the z^{-1} circuit. The pseudo-differential time register has the biggest input range that handles small registration time error. The elimination of clock feedthrough phenomena leads to small time registration errors. Considering the types of conventional and drain-controlled discharging transistor time registers, the input range that handles small registration time error is reduced dramatically. This result comes from the behavior of the transistors that act as switches in the discharging sub-block which lead to big voltage transitions and important clock feedthrough phenomena, affecting the error of individual time registers and finally the input range of z^{-1} operator.

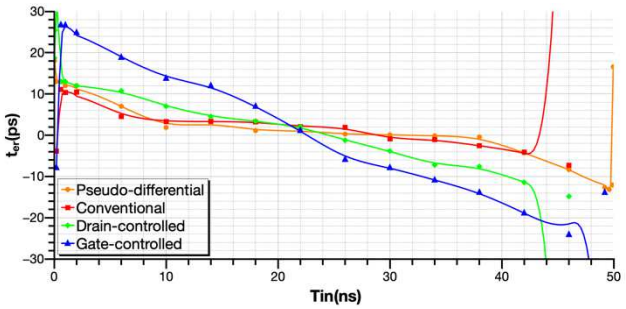

Fig. 9. Absolute error of z^{-1} operator versus all the available input range

As long as the input range is less than $T_{in.max}$ the error τ_{er} of z^{-1} operator is not affected by the clock feedthrough phenomena, but the important factor is the current leakage. The current leakage, when the output is disconnected from the ground is almost identical and that's why the error variation is similar between the different types of time register. The error variation is coming from the different current leakage between the cascaded time registers of z^{-1} operator because the time registers experienced different T_{in} pulse widths on their input. The absolute time error of the z^{-1} operator in relation to input range for each time register topology is presented in TABLE II.

TABLE II. ABSOLUTE TIME ERROR OF Z^{-1} OPERATOR

τ_{er}(ps)			
Topology \ T_{in}	90%$T_{in.max}$	95% $T_{in.max}$	99% $T_{in.max}$
Conventional	6.3	307.3	127
Drain-controlled	12.5	358.7	741.3
Gate-controlled	21.45	21.38	287.43
Pseudo-differential	7.9	11.9	12.8

B. Signal-to-distortion ratio (SDR) of z^{-1} operator

The *SDR* was measured via the comparison of the power of the fundamental frequency to the power of the first ten orders of harmonics of the reconstructed output signal V_{out} as described in eq.(15). The comparison was achieved using the testbench that presented in Fig. 8.

$$SDR = 10log \frac{\sqrt{V_{out.f_0}^2}}{\sqrt{V_{out.f_1}^2+V_{out.f_2}^2+\cdots+V_{out.f_{10}}^2}} \quad (15)$$

In Fig. 10 is illustrated the *SDR* versus $T_{in.peak}$ for $T_{in.peak}$ between 0 and 25ns. Time register with drain-controlled discharging transistor and the pseudo-differential topologies achieve better *SDR* than using the other types of time registers. This is achieved because the voltage V_{GS} of their current sources is constant in a period of a *SET* signal. On the other hand, the voltage V_{GS} of the current source on the conventional topology is depended on the state of the transistor M_2. If M_2 is OFF the current source is disconnected from ground and its voltage is near to V_{cap} and if M_2 is ON then the connection of current source with the ground is leading to a downgrade of its source voltage. Similarly, in the time register with gate-controlled discharging transistor procedure, the voltage V_{GS} of its current source is controlled from the TR_{in} signal resulting to values of the gate voltage of the current source equals to *CTRL* signal or to the ground. This transient of the current source input voltage leads to a more multi-harmonic discharging current, degrading SDR.

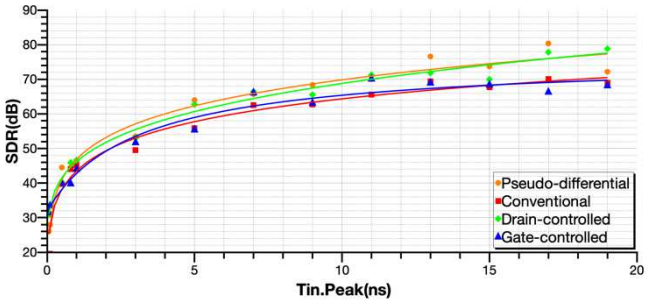

Fig. 10. Signal-to-distortion ratio versus $T_{in.peak}$ in relation to time register types

C. Power consumption

The power consumption of a z^{-1} was measured in respect to a period of *SET* signal. The power consumption of z^{-1} operator using the types of conventional, drain-controlled and gate-controlled time registers is almost equal because the time period of the *SET* signal that the output is connected to the supply is identical and represents the 25% of the *SET* signal. In contrast, the power consumption of the pseudo-differential time register is three times larger than the previous types due to the connection of the output to the supply for at least 50% of the period of a *SET* signal. A performance comparison summary for every type of time register is presented in TABLE III.

TABLE III. Z^{-1} OPERATOR PERFORMANCE SUMMARY

Topology	Performance results of Z^{-1} operator		
	T_{in} (ns)	SDR_{max} (dB)	Consumption (uW)
Conventional	45.4	70.1	11
Drain-controlled	45.4	78.8	10.3
Gate-controlled	49	70.2	10
Pseudo-differential	49.5	80.3	28.4

VI. CONCLUSIONS

In this work, a comparison study has been done between different types of time registers under a z^{-1} implementation in respect to absolute error, signal-to-distortion-ratio and power consumption. The z^{-1} implementation using conventional time registers offers low power consumption and small absolute error in a specific range of magnitude of T_{in}. The gate-controlled discharging transistor time registers achieves also low power consumption and small absolute error for a wider range of magnitude of T_{in} than the previous option. However, the implementations with these two types are degrading the SDR maximum levels. The implementation using drain-controlled discharging transistor time registers improves the SDR maximum levels, consumes almost identical power from the supply as the previous types, but with a cost of a smaller input range where it achieves low absolute error. Lastly, the pseudo-differential z^{-1} operator achieves the widest input range in which the absolute error is small and, high SDR maximum levels. However, the last option raises significantly the power consumption of the z^{-1} operator.

All time register types have pros and cons and therefore the more suitable type should be chosen according to the overall system requirements. If a system requires a low power design, gate-controlled option is the best one choice due to its' large input range and small power consumption. On the other hand, if the linearity performance is mandatory the pseudo-differential time register type is the best candidate to achieve low absolute error for a wide input range and small harmonic distortion.

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